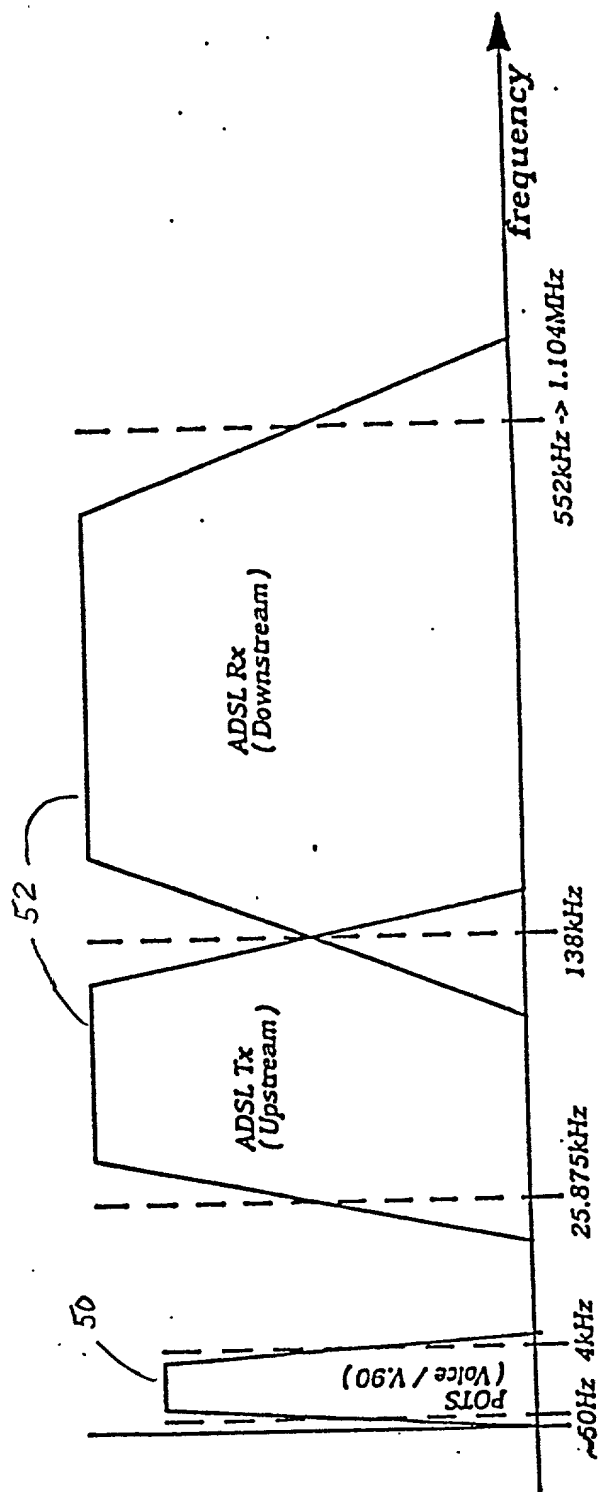


Prior Art

Fig 1



Prior Art

Fig 2

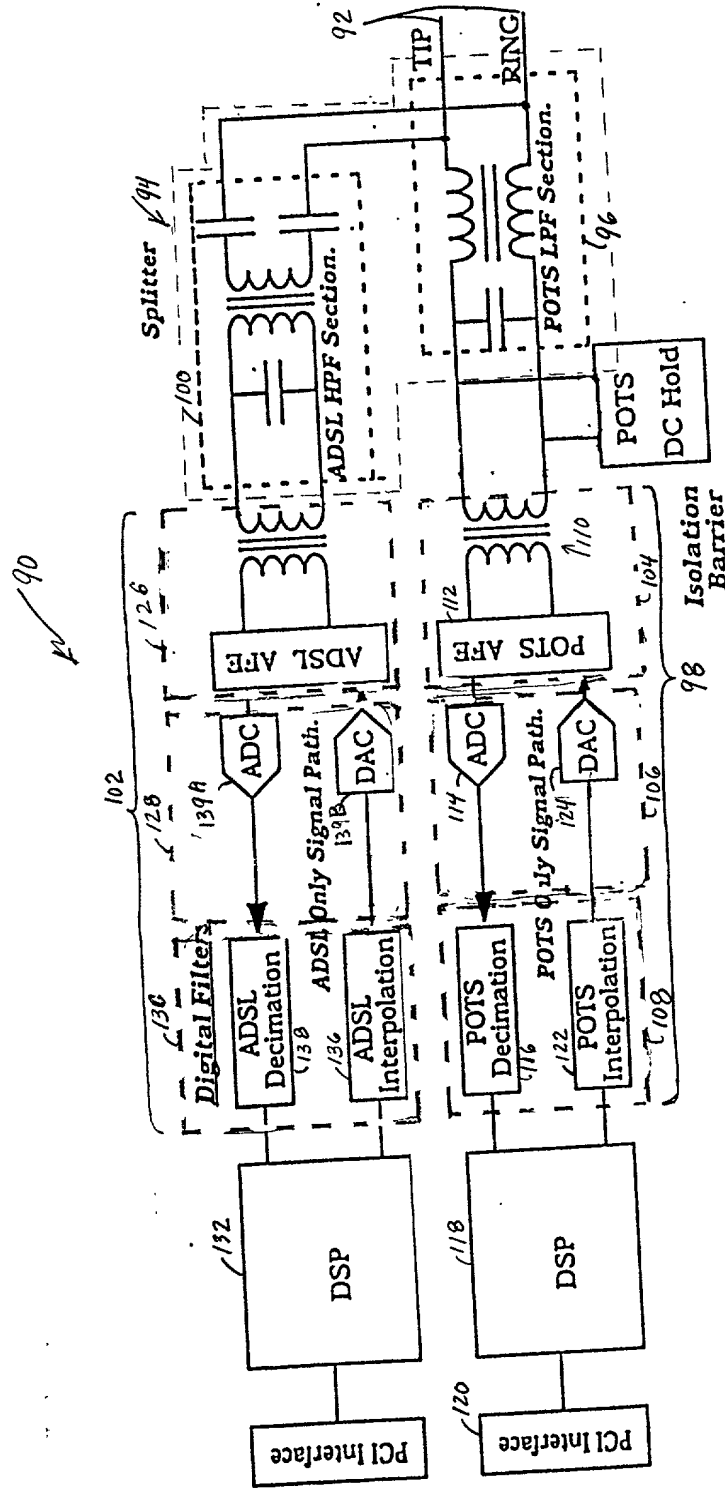


Fig. 3 Prior Art

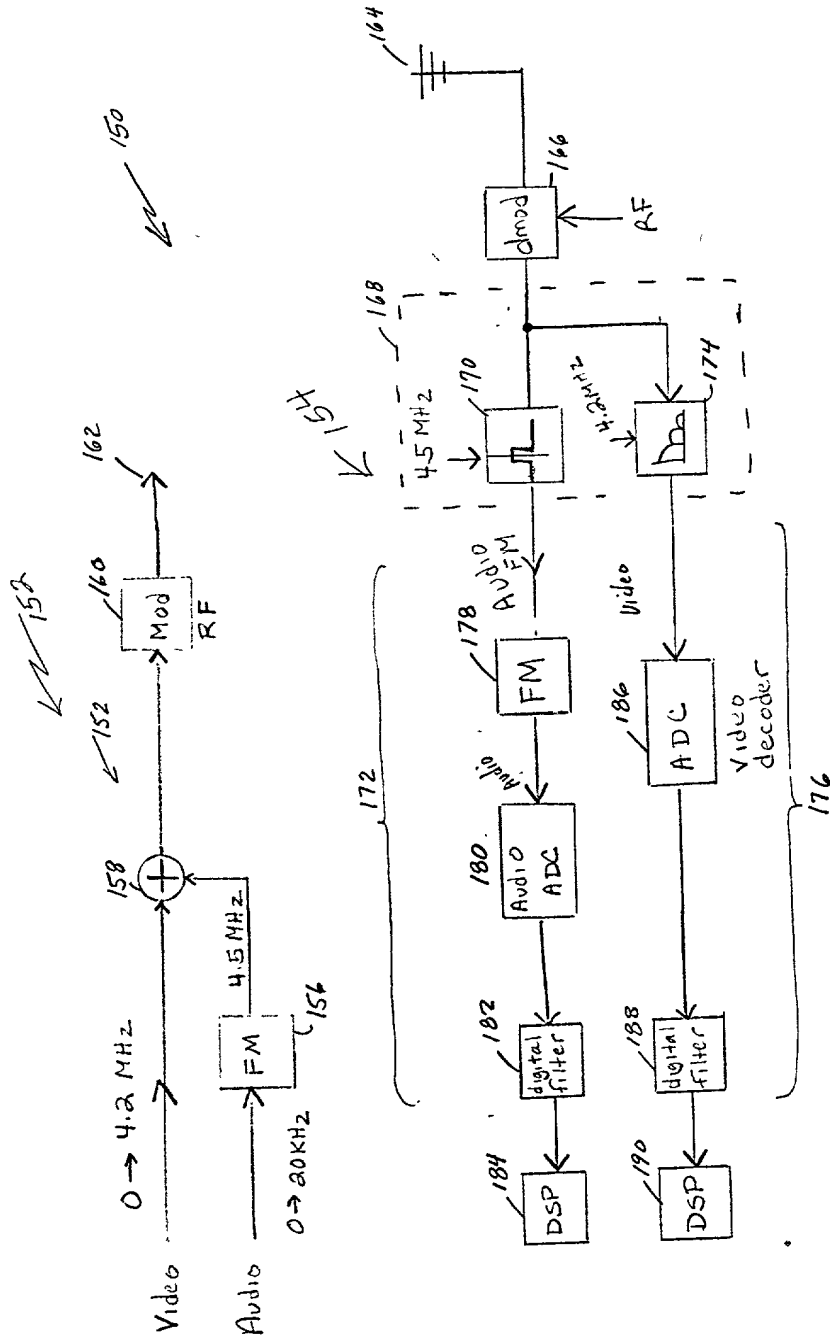


Fig 4 Prior Art

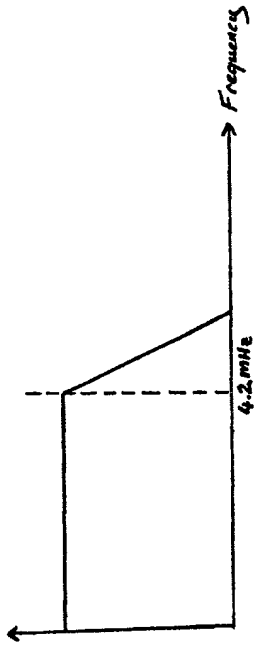


Fig. 5 Prior Art

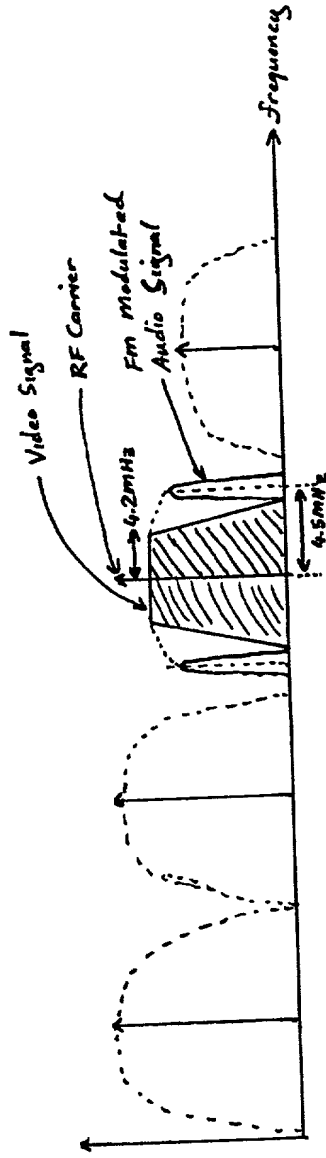


Fig 6 Prior Art

FIG. 7 is a block diagram of a prior art echo canceller system.

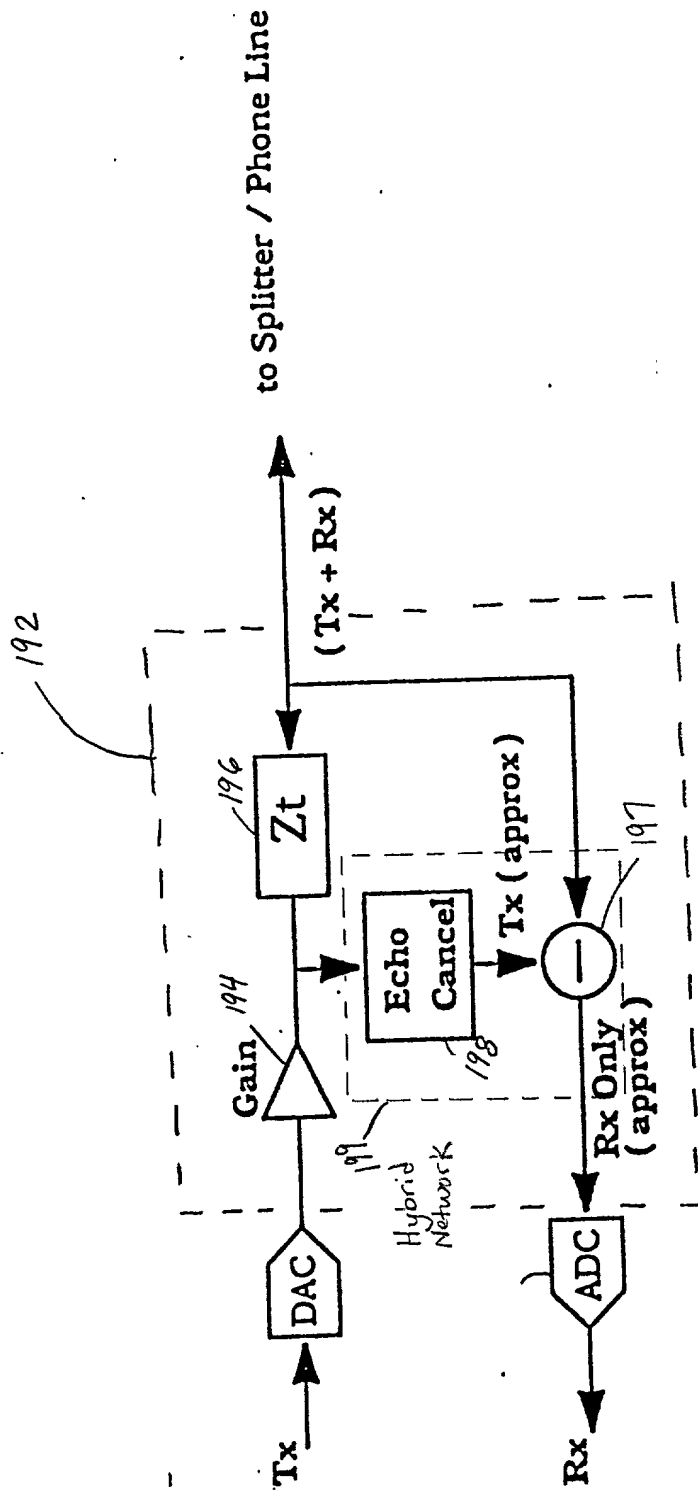


Fig. 7 Prior Art

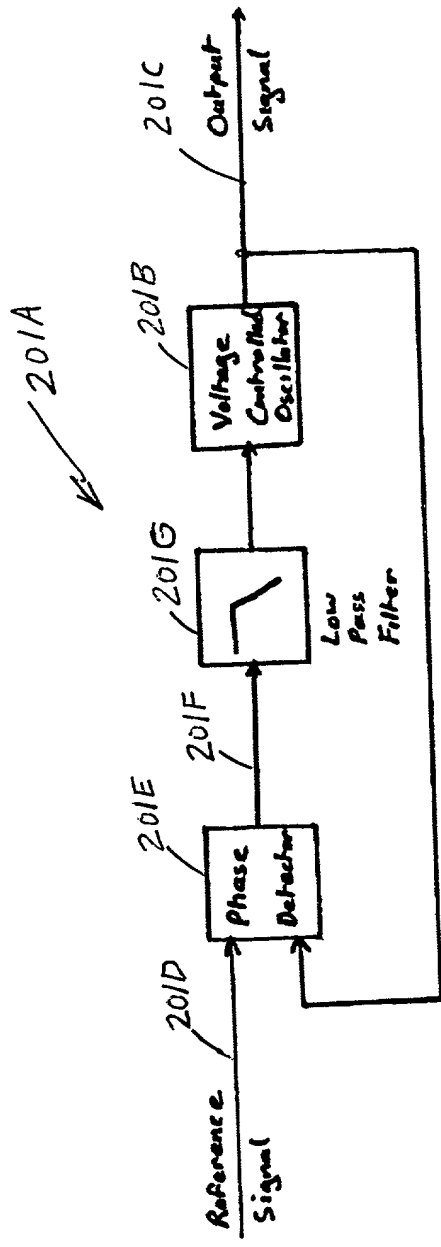


Fig 8 Prior Art

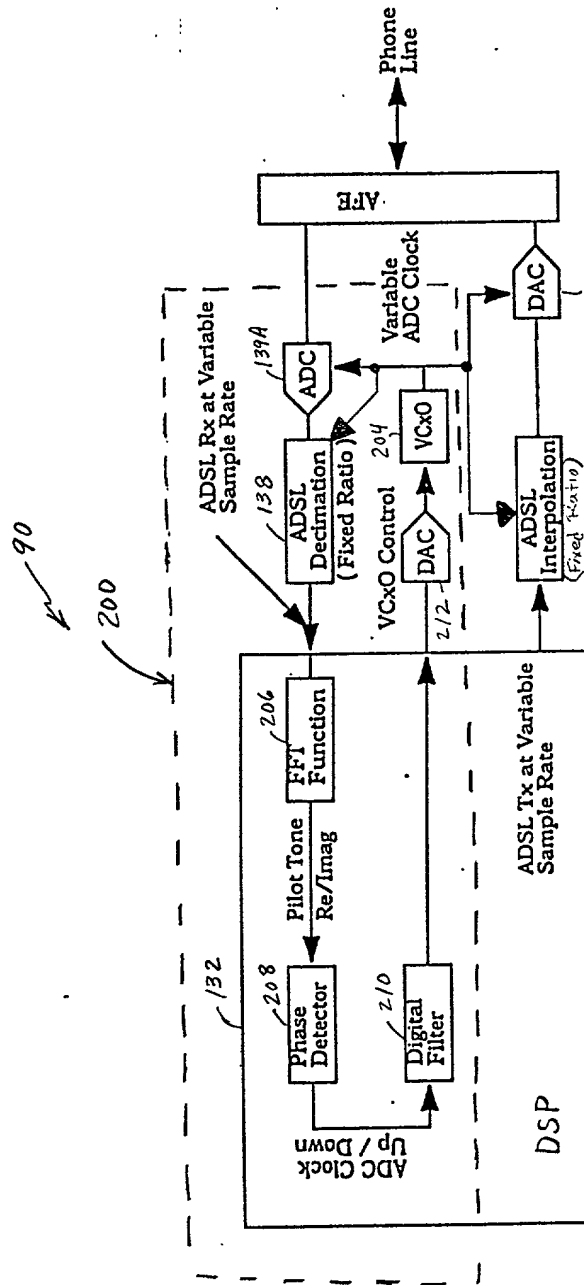


Fig. 9 Prior Art

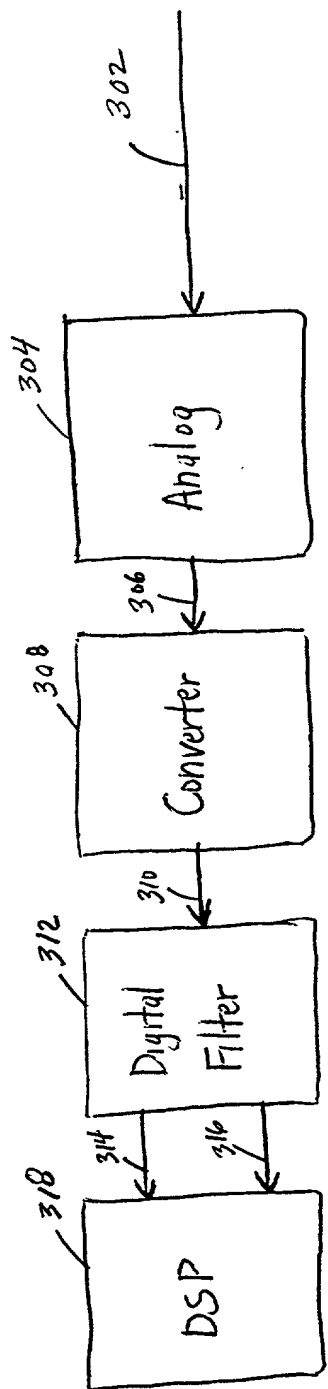


Fig. 10

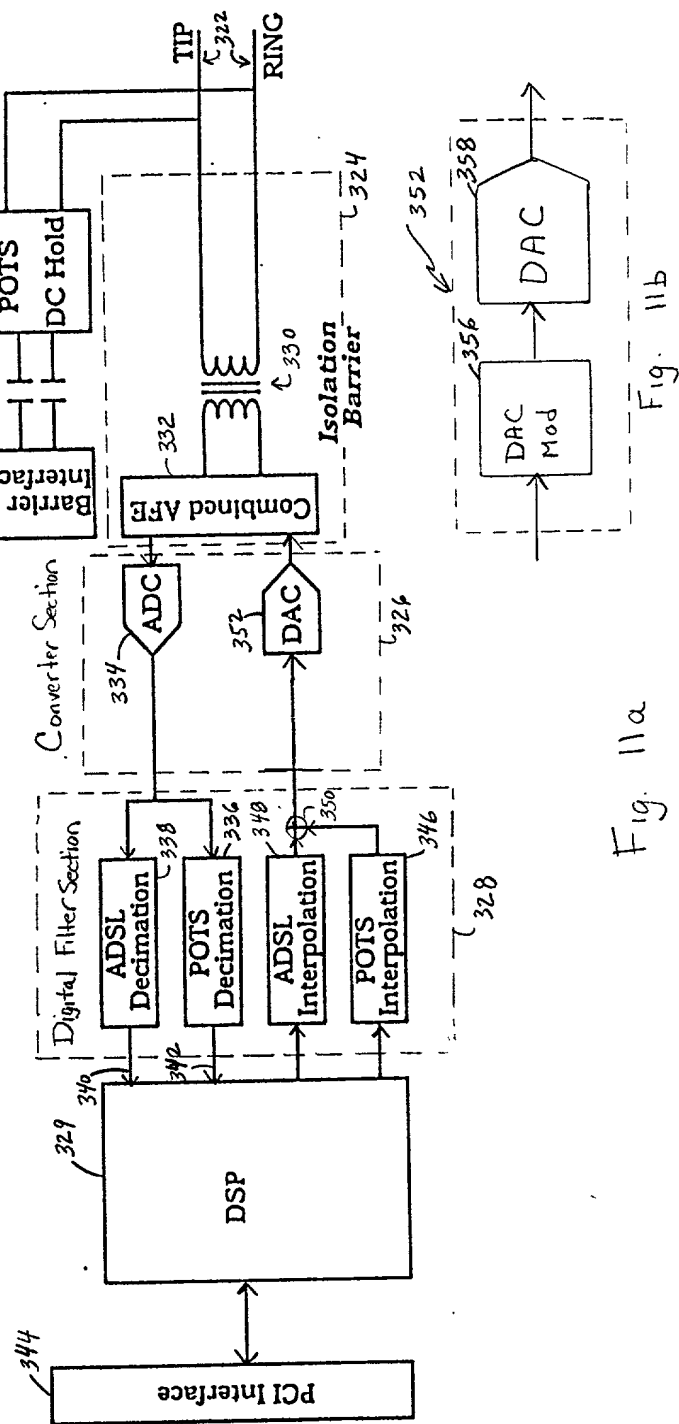
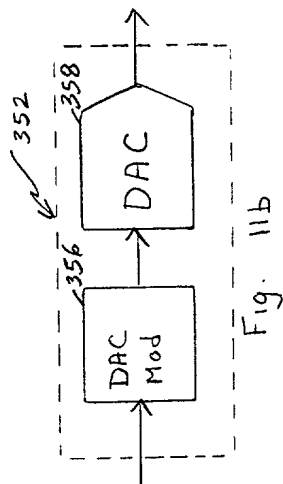


Fig. 11a



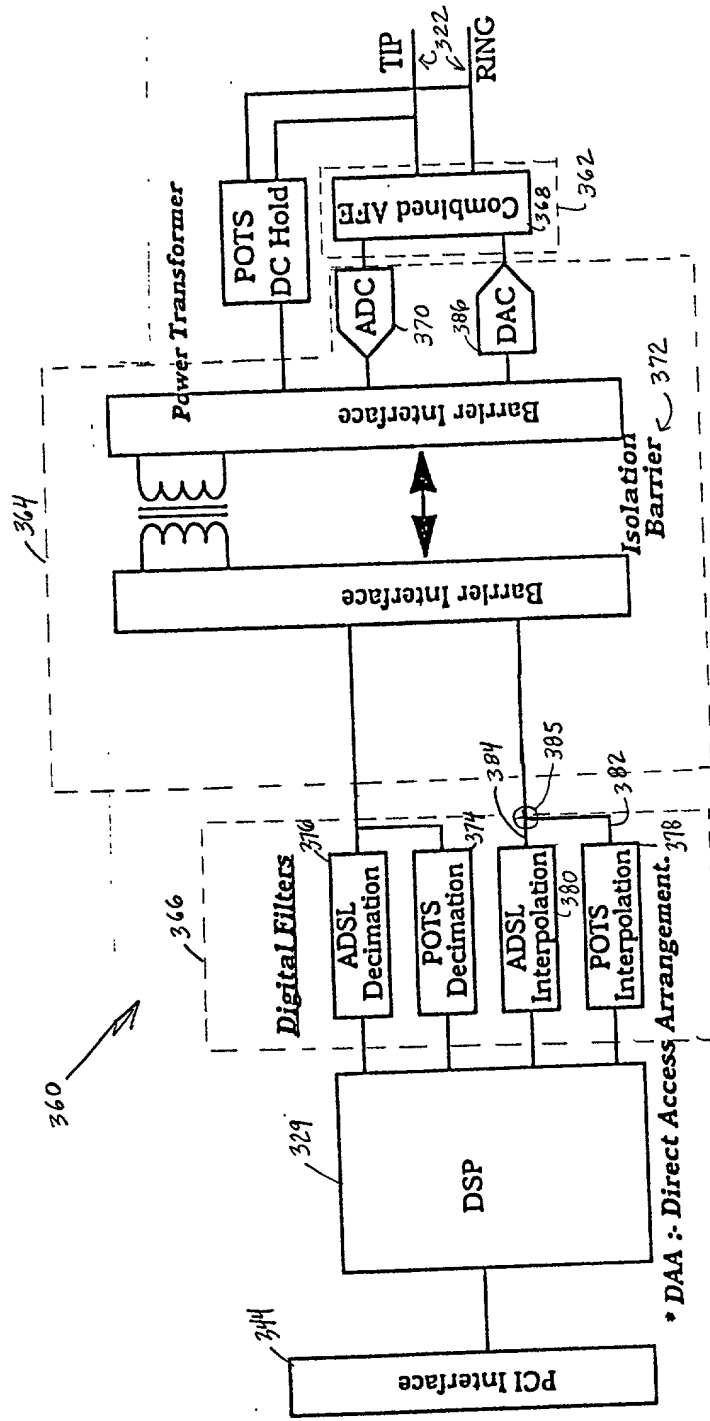


Fig. 12a

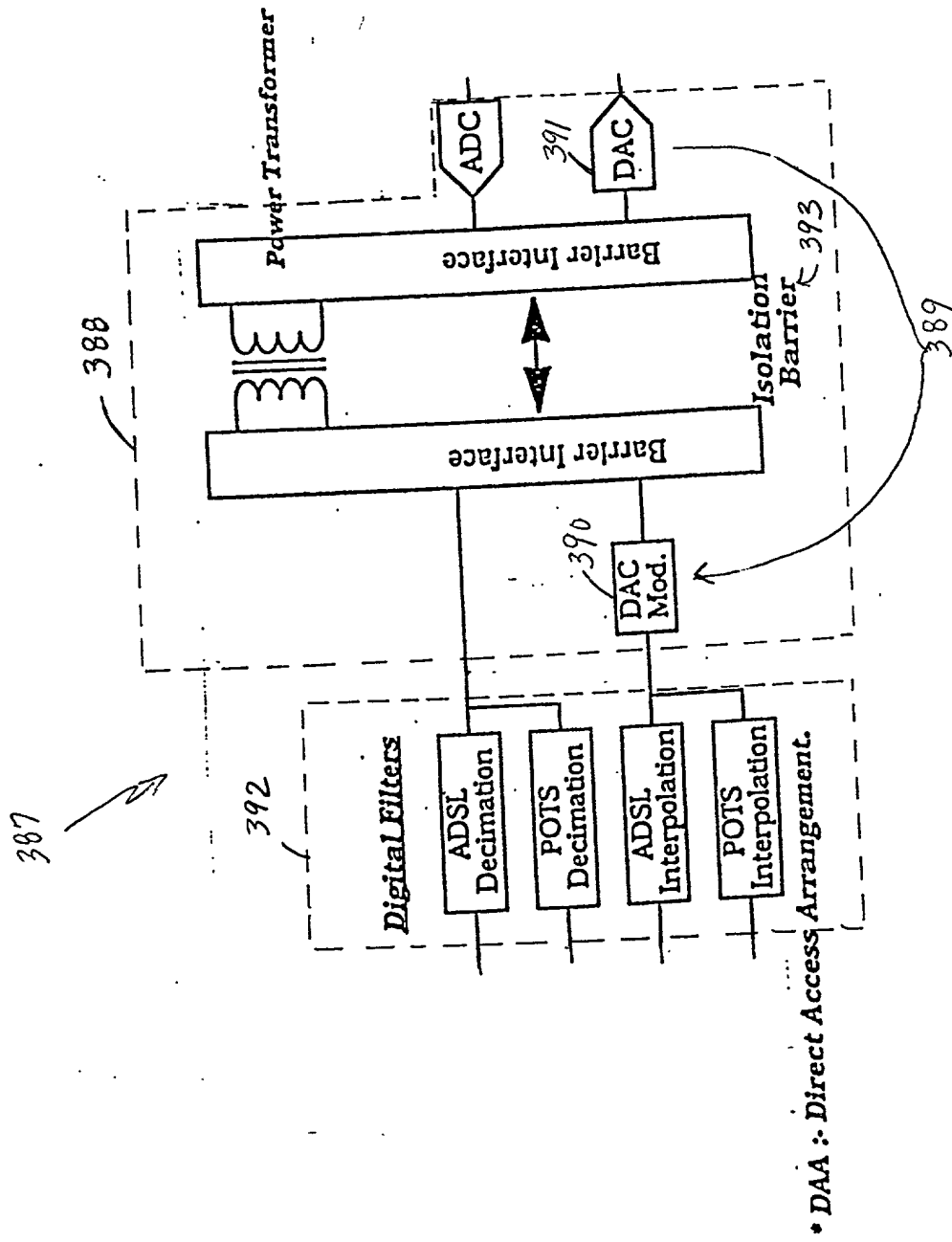


Fig. 12b

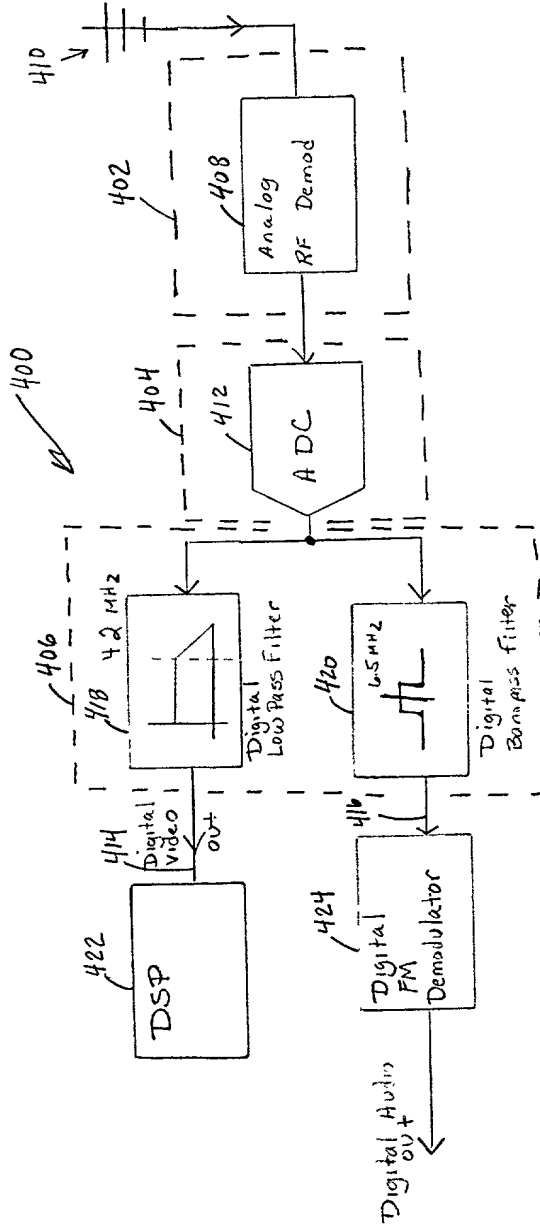


Fig. 13

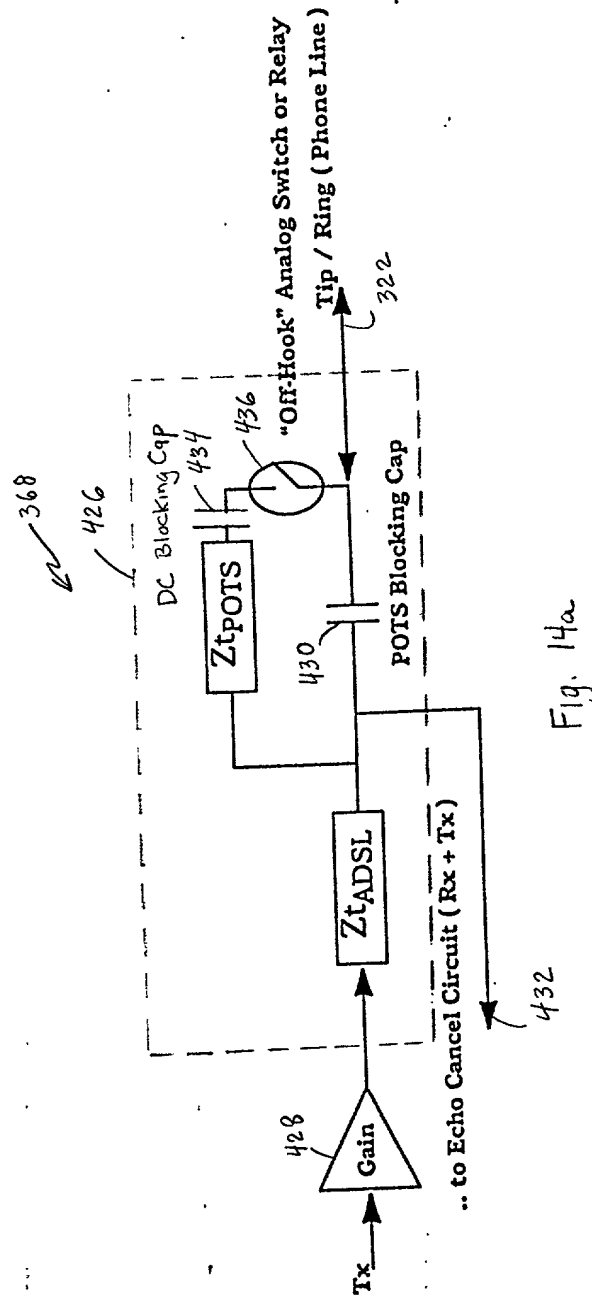


Fig. 14a

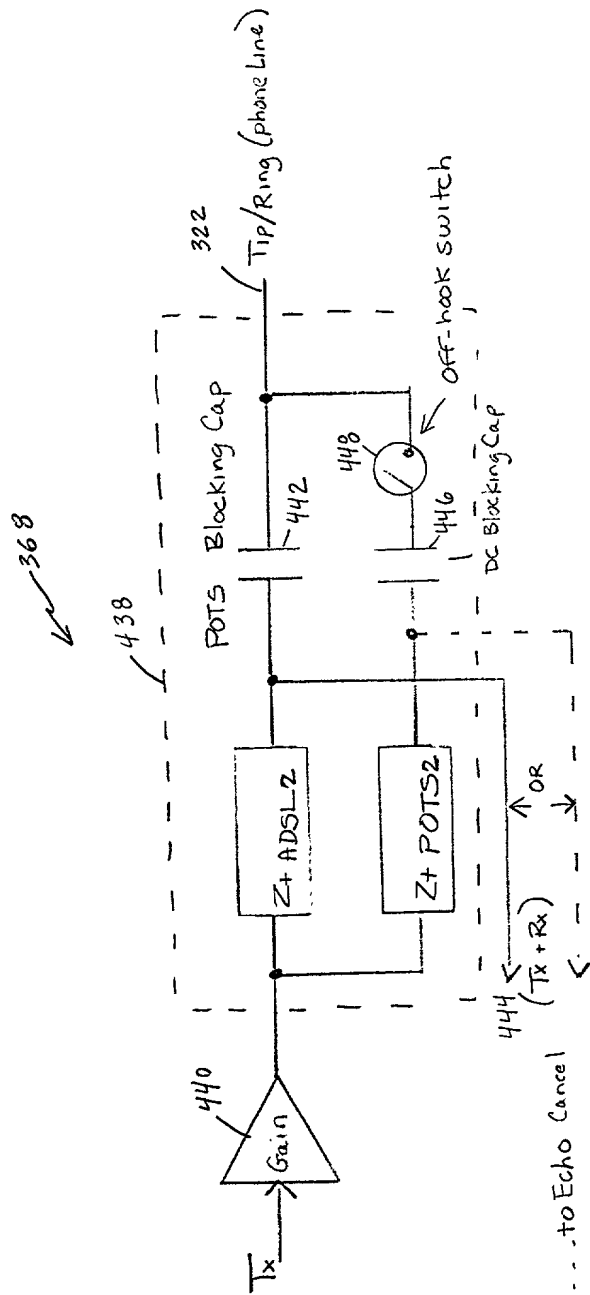


Fig 14b

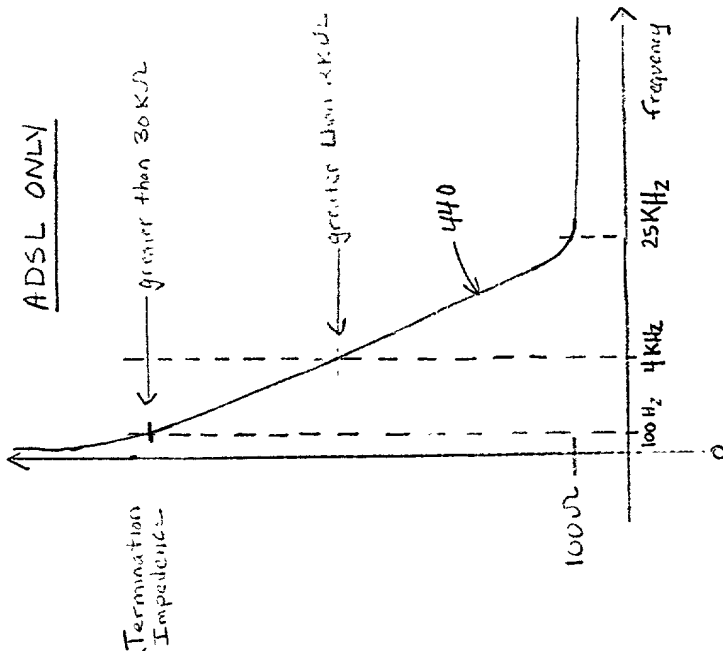


Fig 15a

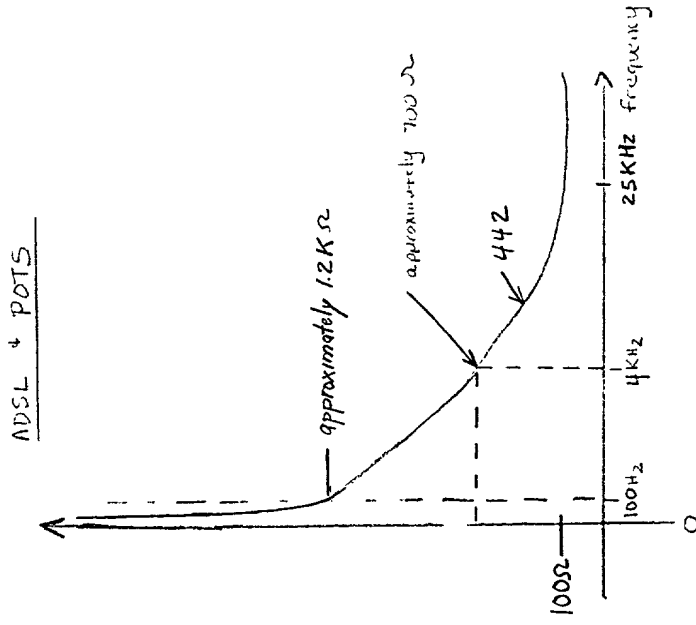


Fig. 15b

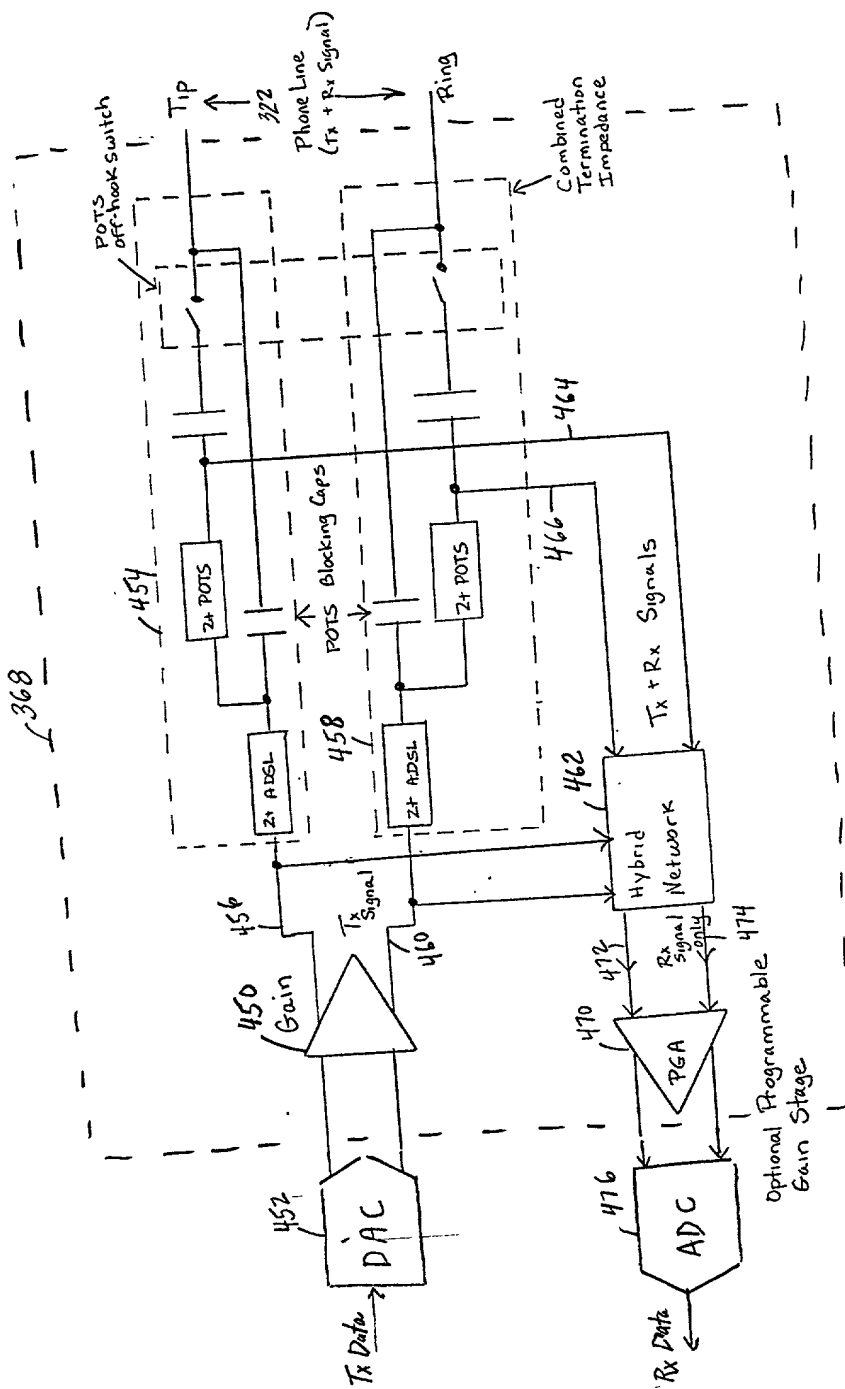
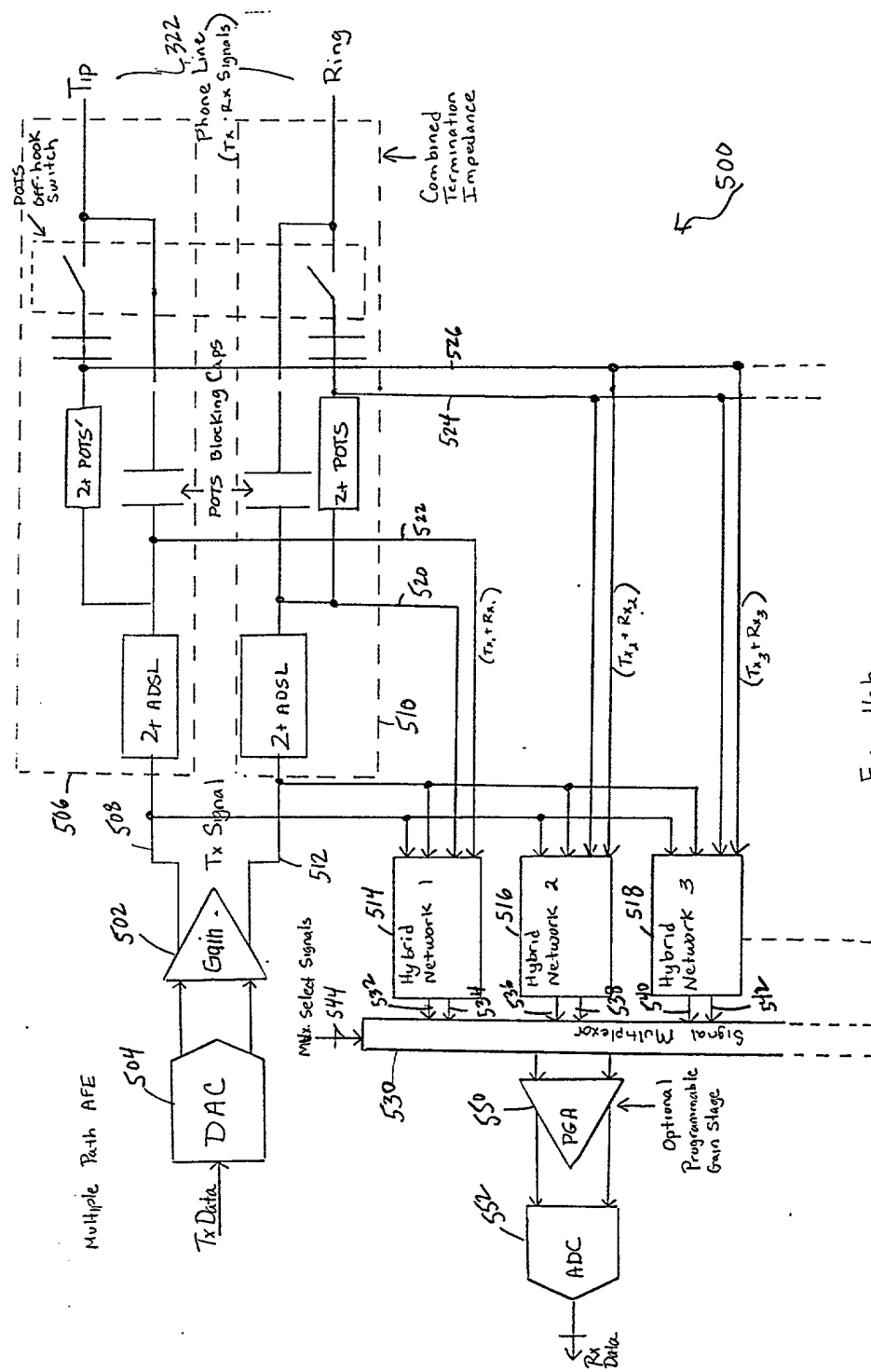


Fig 16a



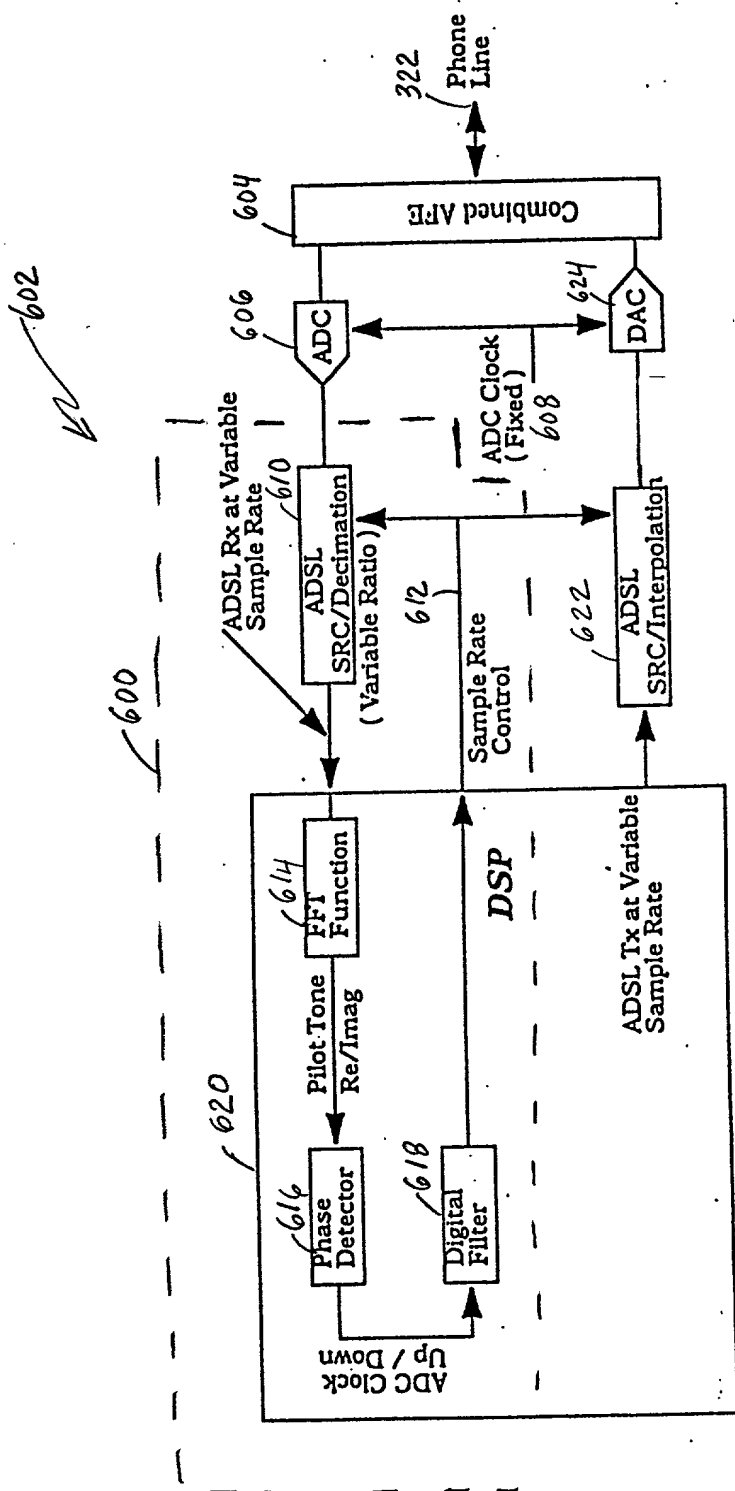


Fig. 17

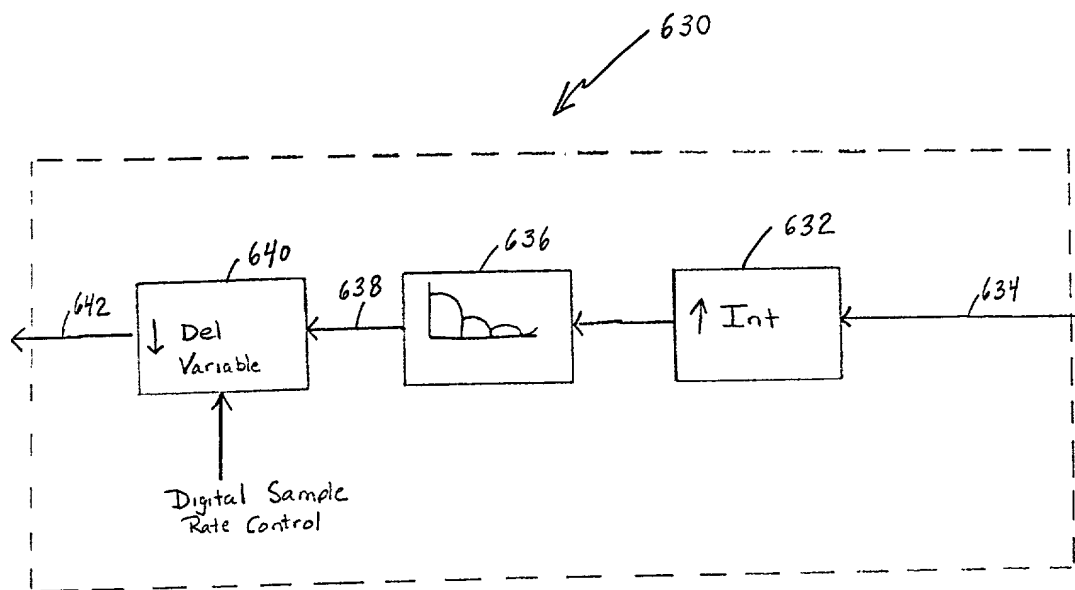


Fig 18

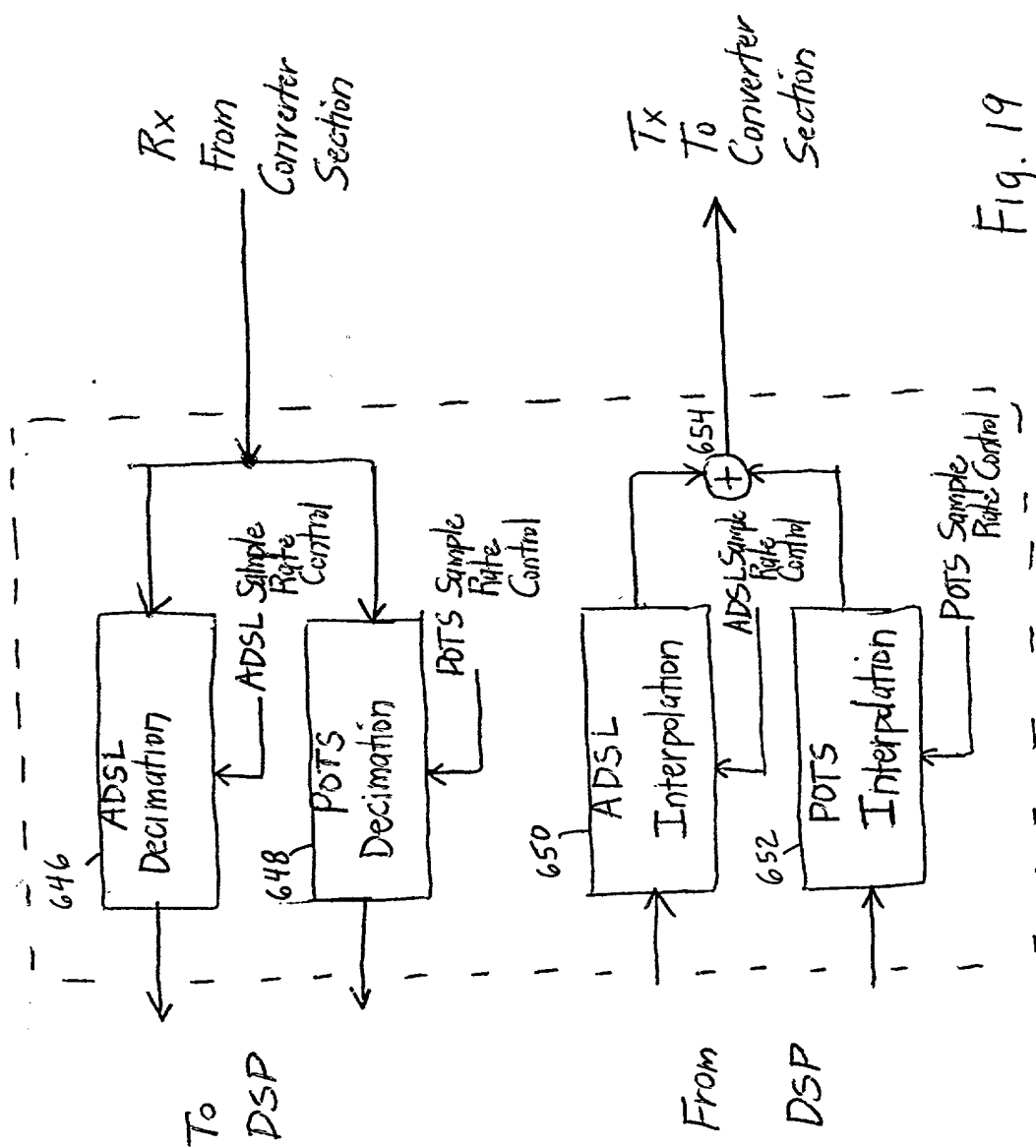


Fig. 19

FIG. 20a is a block diagram of a digital signal processing system for an ADSL transmitter. The system includes a 1.104 MHz ± 400 PPM clock source, an ADSL Tx Data Stream input, and a 552 kbit/s ± 400 PPM clock input. The system is divided into two main paths: an ADSL Transient Interpolation Path and a POTS Transient Interpolation Path. The ADSL path includes a series of blocks labeled 742, 744, 746, 748, 750, 752, 754, 756, 758, and 760, with a variable gain block. The POTS path includes a series of blocks labeled 720, 722, 724, 726, 728, 730, 732, 734, and 736, with a variable gain block. The outputs of both paths are summed at block 740 and then fed into a DAC Data input at block 742. The DAC output is a 4-bit signal at 8.192 MHz, which is then processed by a Σ-Δ Mod block (746) and a 4x up-sampler (748) to produce the final output at block 750.

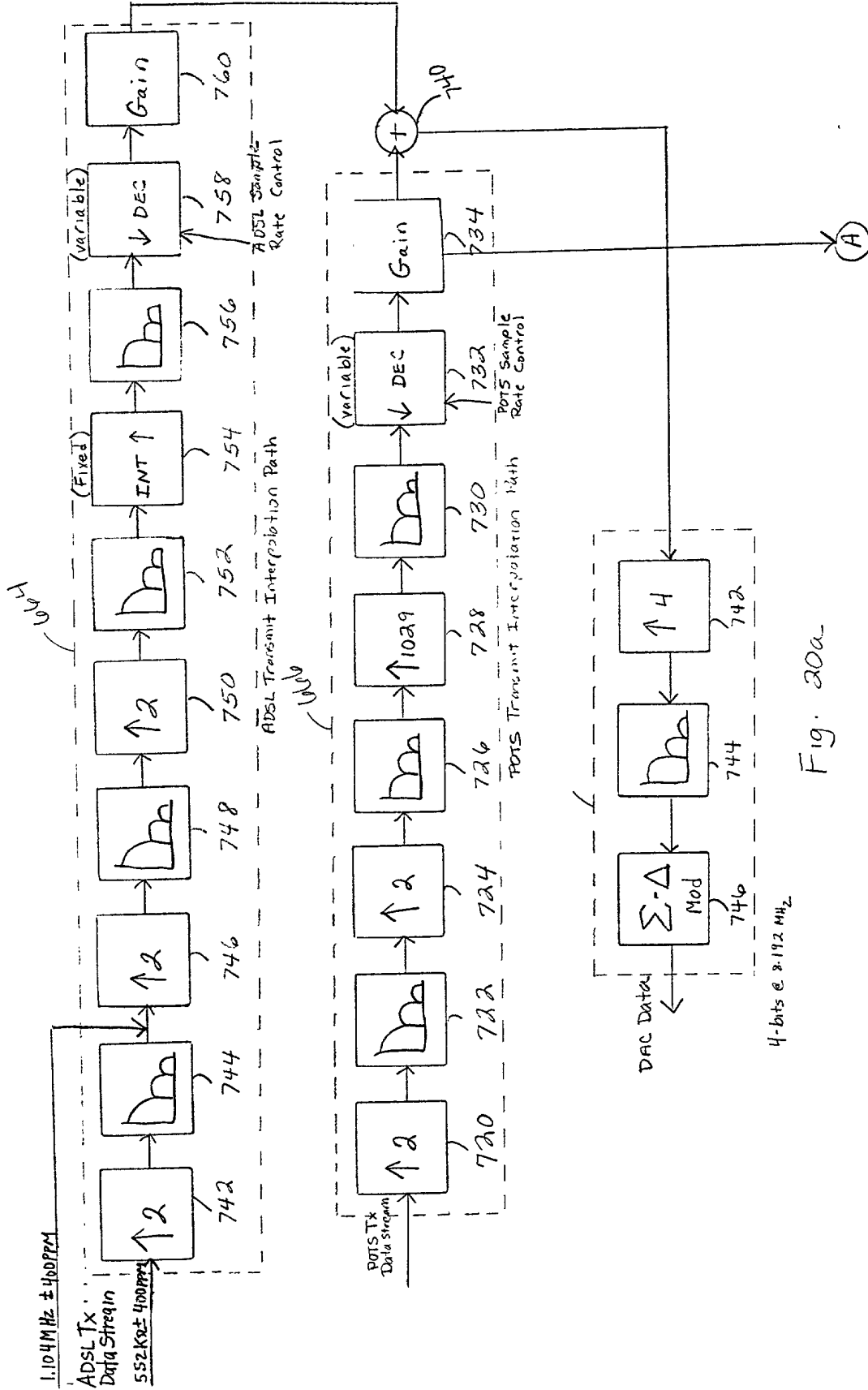


Fig. 20a

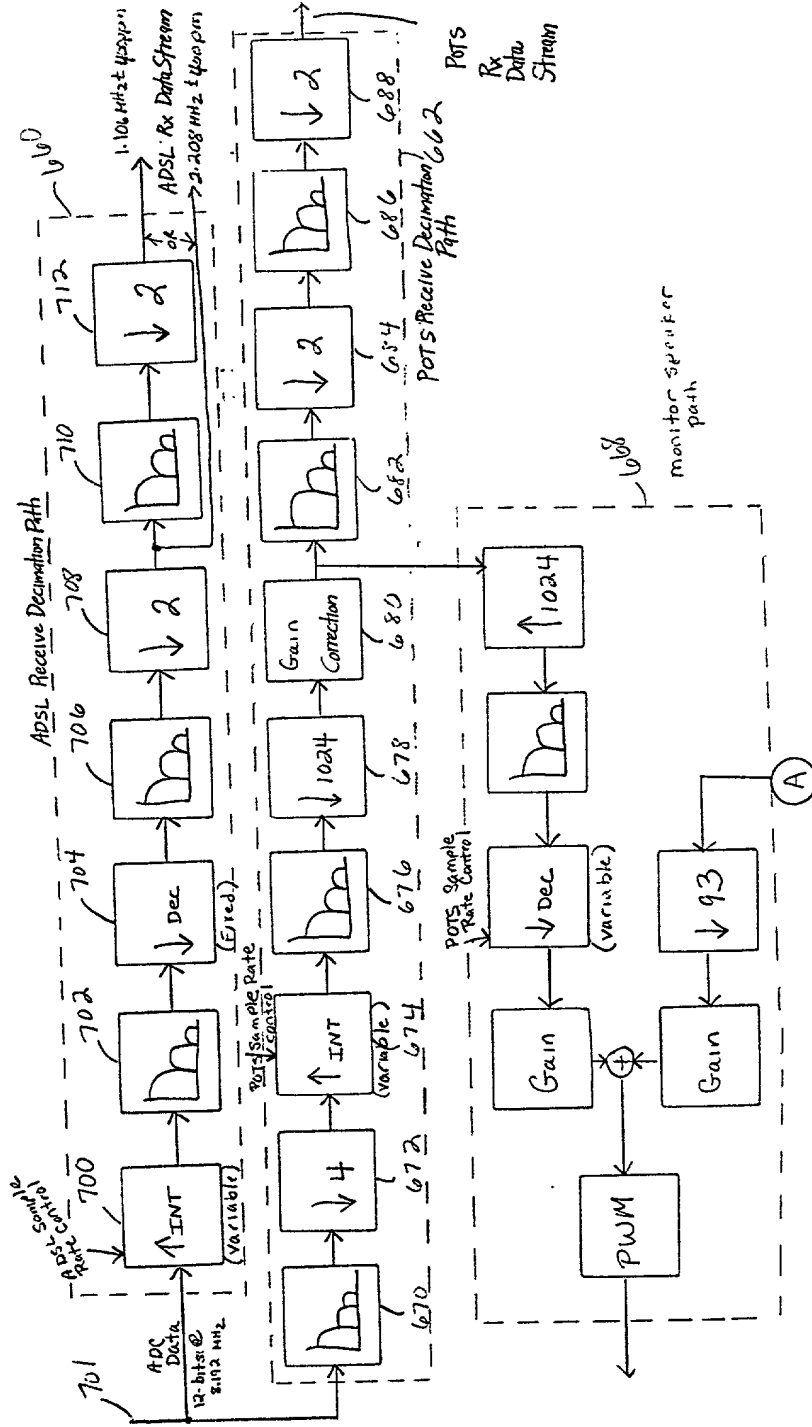
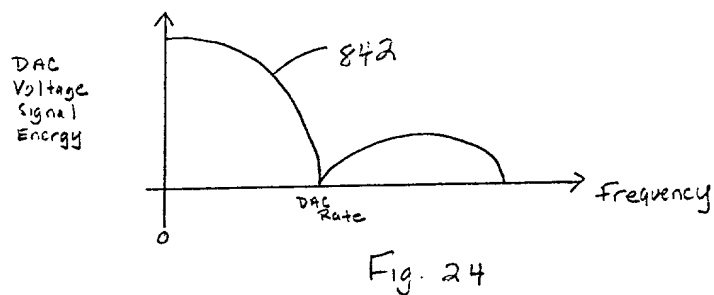
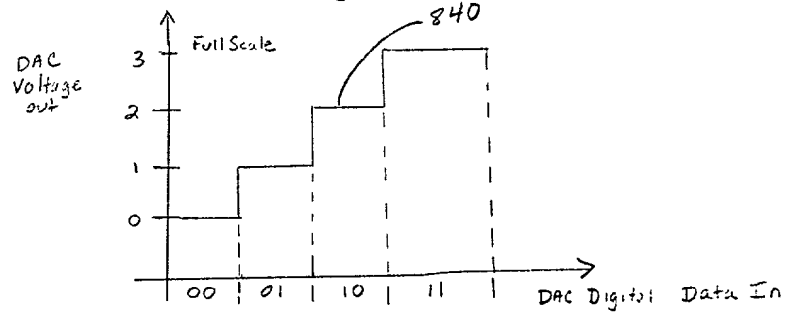
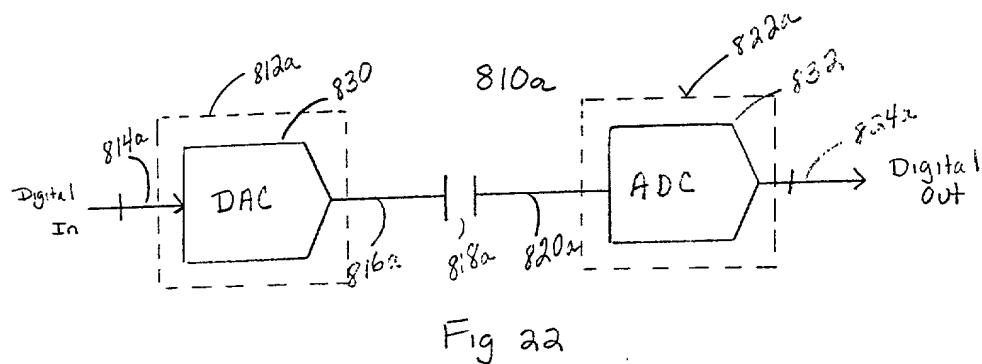
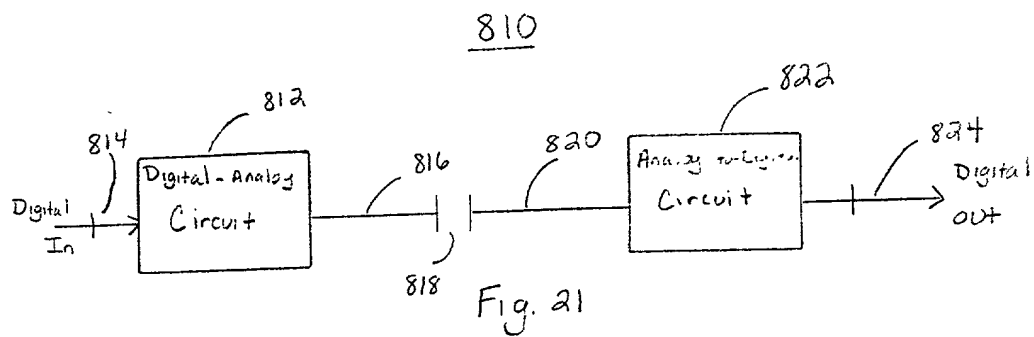


Fig 20b



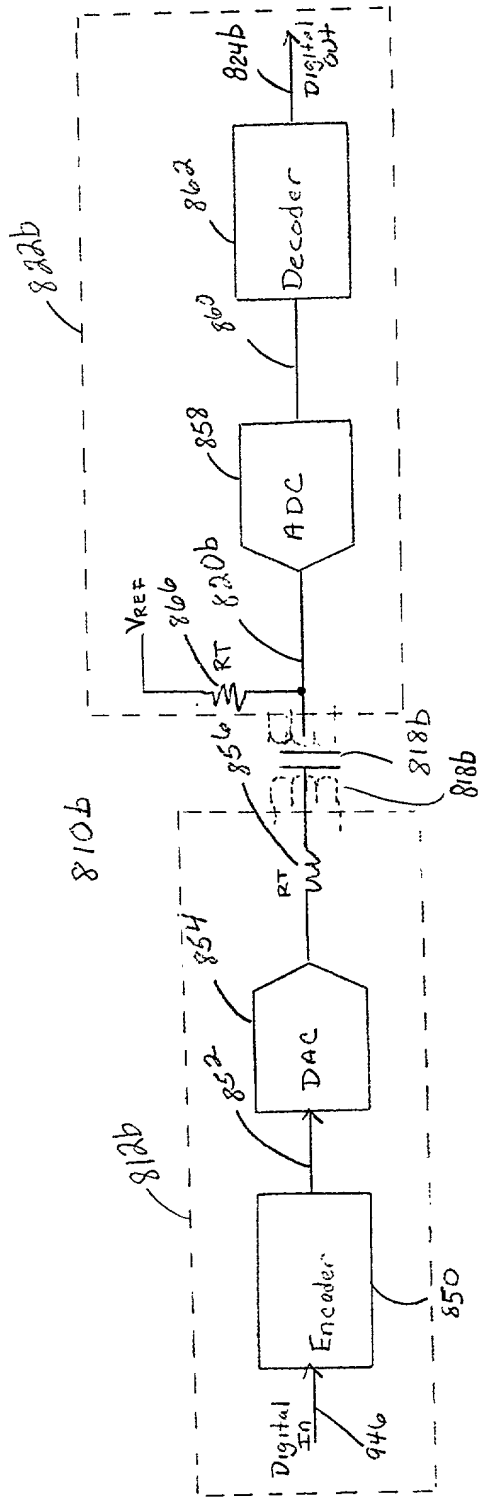


Fig 25

# ENCODER

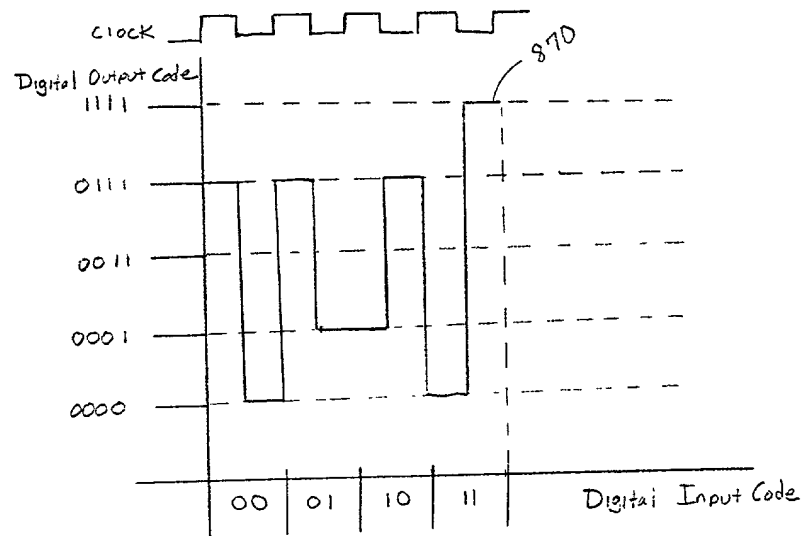


Fig. 26

DA2

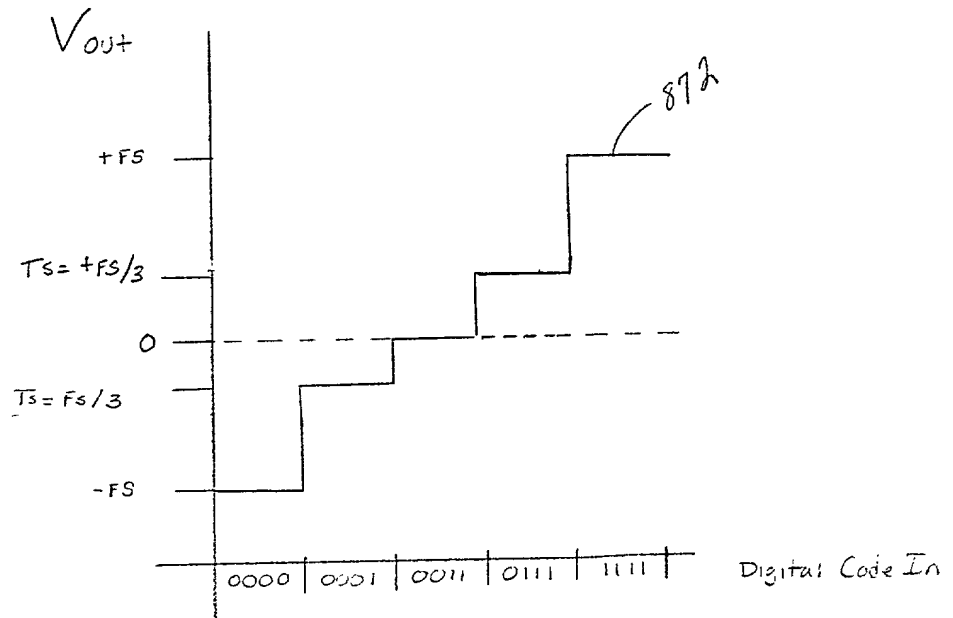


Fig. 27

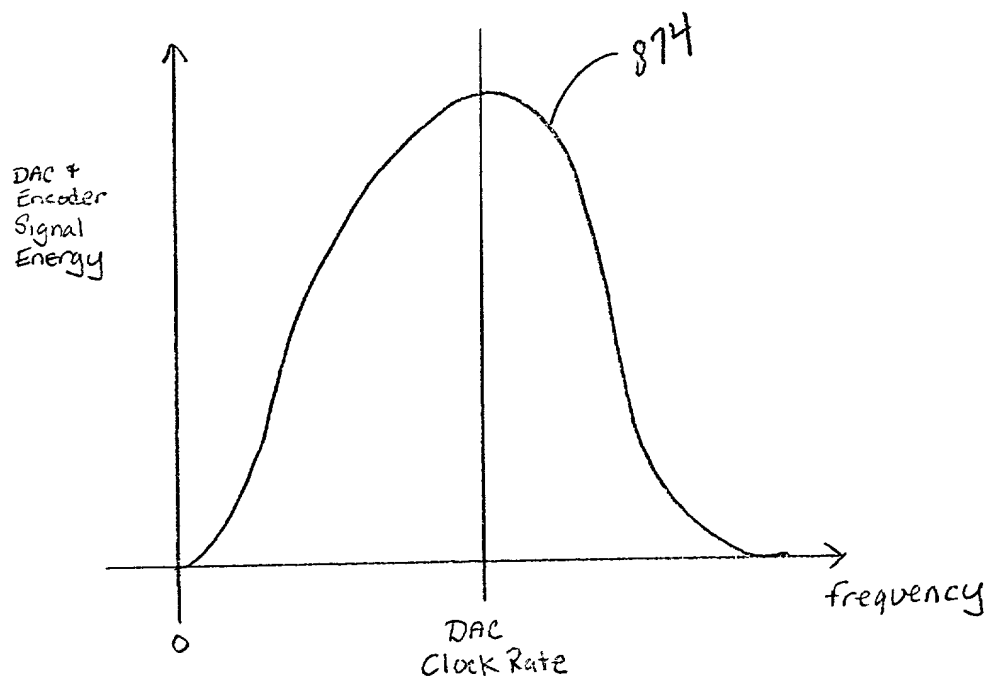


Fig. 28

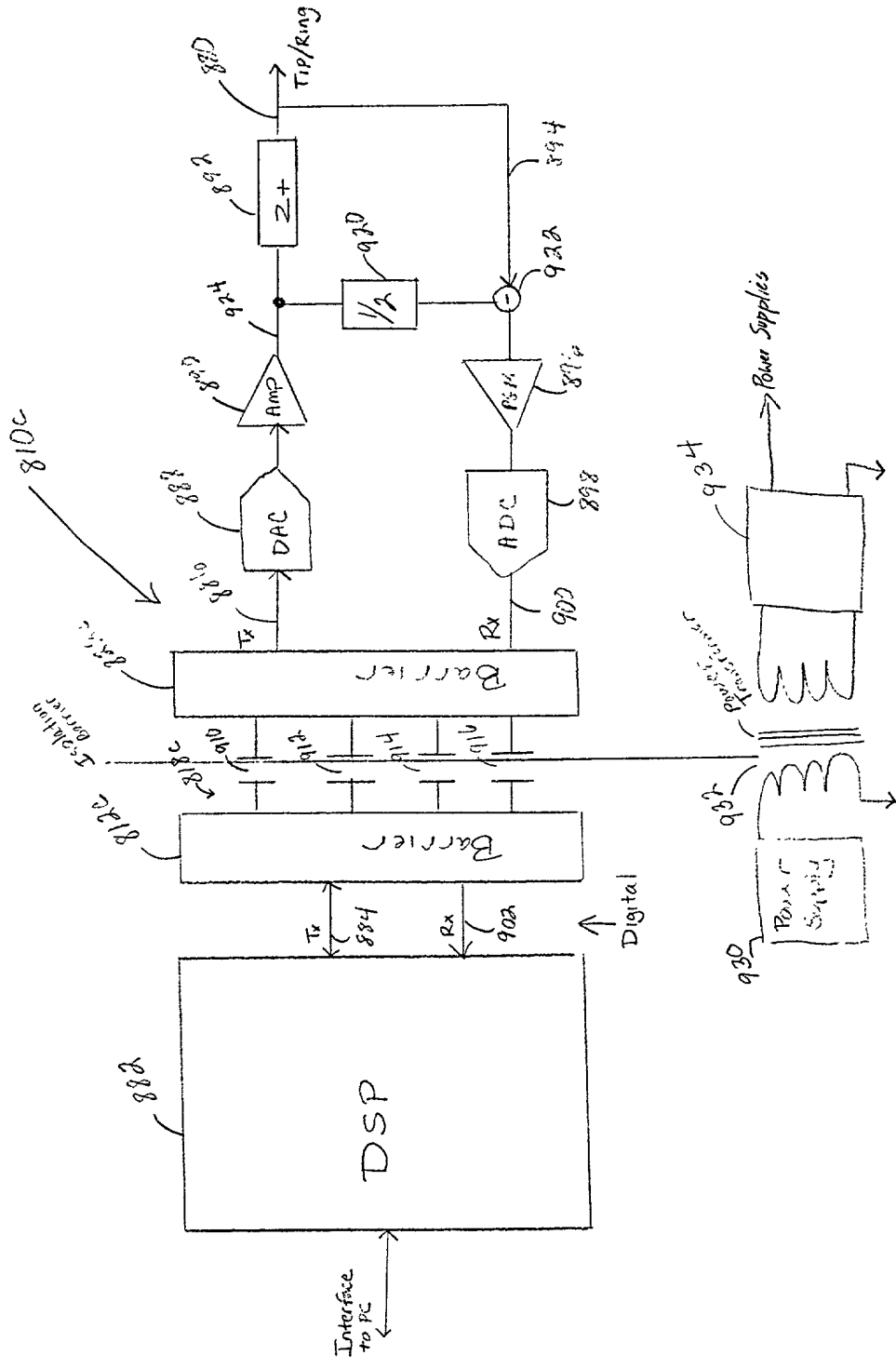


FIG. 8

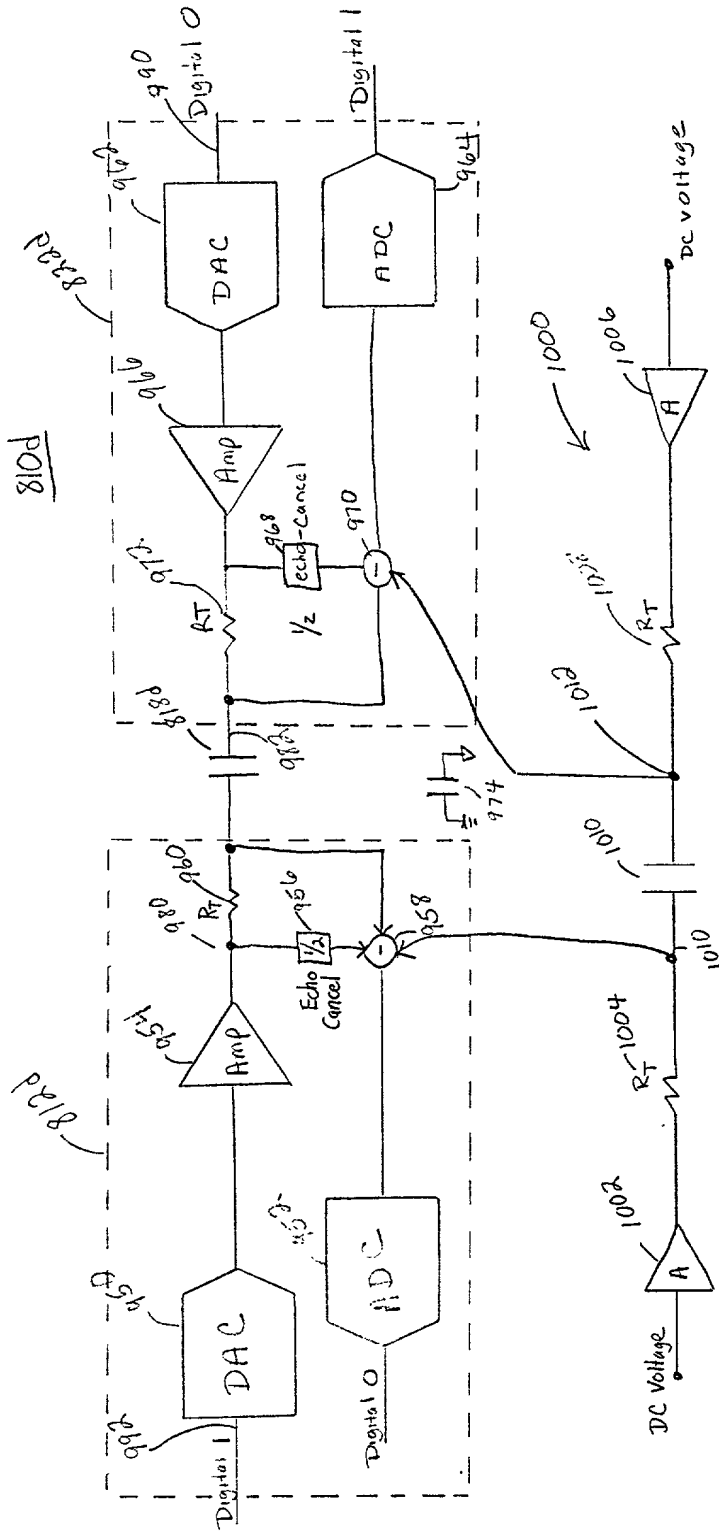


Fig 30

# Full Barrier System

810e

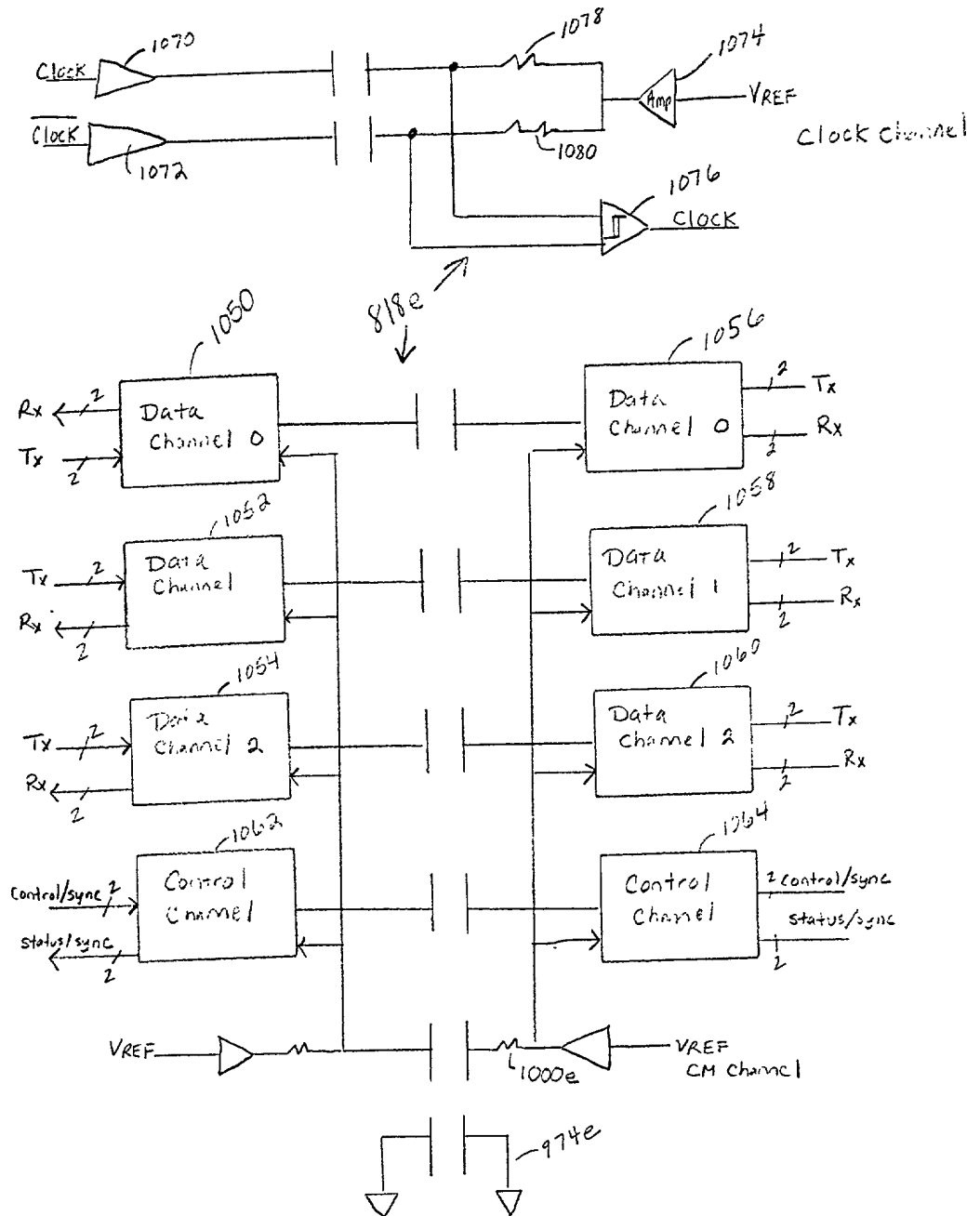


Fig. 31

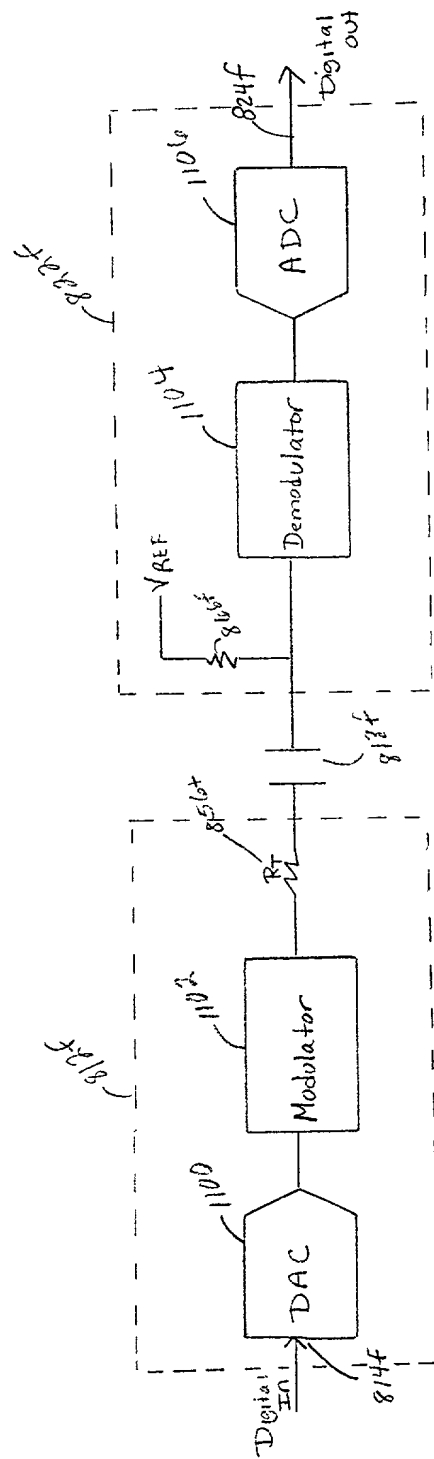


Fig. 32